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10/694,005	10/28/2003	Yojiro Matsueda	117554	3671

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EXAMINER	
BODDIE, WILLIAM	
ART UNIT	**PAPER NUMBER**
2629	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/26/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/694,005	MATSUEDA ET AL.	
	Examiner	Art Unit	
	William L. Boddie	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 February 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8,11-15,20-24,26 and 30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,11-15,20-24,26 and 30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. In an amendment dated, February 1st, 2007, the Applicant amended claims 1-2, 5, 7, 11, 13, 20, 22-24 and 26. The Applicant also cancelled claims 16-19 and 27-29. Currently claims 1-8, 11-15, 20-24, 26 and 30 are currently pending.

Continued Examination Under 37 CFR 1.114

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on February 1st, 2007 has been entered.

Response to Arguments

3. Applicant's arguments filed February 1st, 2007 have been fully considered but they are not persuasive.

On pages 11-12 of the Remarks the Applicants argue that Ohtaka does not disclose a series of electro-optical elements that end substantially simultaneously. The Applicants further argue that the limitation of ending substantially simultaneously is referring to the series of electro-optical elements, and not the duration of the sustaining period.

The Examiner must respectfully disagree. As the independent claims are presently constructed, it is the plurality of sub-frames that must end substantially simultaneously. Grammatically it currently appears that the claim phrasing at question

could be reworded as follows: The plurality of sub-frames end substantially simultaneously. Furthermore the plurality of sub-frames are set for a series of electro-optical elements among the plurality of electro-optical elements, the series of electro-optical elements being connected to at least two scanning lines.

In short, the location of the commas within the phrase indicate that "end substantially simultaneously" points back to the plurality of sub-frames. It is this interpretation that will be maintained in the current and future Office actions barring rewording of the phrasing.

It should also be mentioned that Ohtaka does seem to disclose, the Applicant's interpretation of the phrase. Ohtaka clearly discloses in claim 4 a matrix of pixels, each with electro-optic elements. It should be readily clear that each row and column ends substantially simultaneously.

Applicant's arguments with respect to claims 1-8, 11-15, 20-24, 26 and 30 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-8, 11-12, 20-24 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohtaka et al. (US 6,151,000) in view of Asano (US 6,975,290).

With respect to claim 1, Ohtaka discloses, an electro-optical device, comprising:

a plurality of scanning lines (27 in fig. 4, for example);

a plurality of sustaining lines (28 in fig. 4, for example);

a plurality of electro-optical elements (col. 1, lines 4-10; col. 4, lines 33-36); and

a plurality of pixels, each of the plurality of pixels having an electro-optical element (col. 1, lines 4-10; col. 4, lines 33-36), brightness of each of the electro-optical elements being set for each of a plurality of sub-frames (col. 4, lines 36-48; fig. 7d), which constitute one frame of a period (1 field is equivalent to one frame in fig. 7d) and each have a predetermined period (clear from fig. 7d), so that at least two levels of brightness can be set for one frame (col. 4, lines 44-48); and

a sub-frame having a longest period among the plurality of sub-frames being divided into a least two allocated sub-frames (SF1 and SF6 in fig. 7d; col. 8, line 62 – col. 9, line 2), and

the plurality of sub-frames, which are set for a series of electro-optical elements among the plurality of electro-optical elements (col. 1, lines 9-10), the series of electro-optical elements being connected to a scanning and sustaining line (note the two x-axis electrodes per pixel in fig. 4), end substantially simultaneously (clear from fig. 7d that the sub-frame sustaining period (grayed area) ends simultaneously).

Ohtaka does not expressly disclose a plurality of data lines, a pixel circuit or connecting two scanning lines to the series of electro-optical elements.

Asano discloses, an electro-optical device, comprising:

a plurality of scanning lines (127 in fig. 4);

a plurality of data lines (133 in fig. 4);

a plurality of electro-optical elements (121 in fig. 3); and

a plurality of pixel circuits (131 in fig. 4) to drive the plurality of electro-optical element, each of the plurality of pixel circuits having a first transistor (124 in fig. 3) and a storage capacitor (123 in fig. 3) to store a data signal (col. 3, lines 23-30) supplied via a data line (128 in fig. 3) among the plurality of data lines and the first transistor (clear from fig. 3); wherein the electro-optical elements are connected to at least two scanning lines (127A-B in fig. 3). Asano further discloses, that the data signal stored in the capacitor sets the brightness of the pixel (col. 2, lines 33-51; also note col. 3, lines 20-29).

Asano and Ohtaka are analogous art because they are both from the same field of endeavor namely driving and control circuitry for electro-optical displays.

At the time of the invention it would have been obvious to one of ordinary skill in the art to replace the addressing and pixel circuitry of Ohtaka with the pixel circuit and scanning lines of Asano.

The motivation for doing so would have been to achieve a high image contrast and high response speed (Asano; col. 1, lines 43-44).

With respect to claim 2, Ohtaka and Asano disclose, the electro-optical device according to claim 1 (see above).

Ohtaka further discloses, the sum of the period of the at least two allocated sub-frames (col. 8, line 29; largest luminous weight is 16, therefore the sum of the two

divided sub-frames is 16) being set to 2^n times as long as a sub-frame having a shortest period (shortest period or smallest luminous weight is 1) among N sub-frames of the plurality of sub-frames, wherein n is a number of sub-frames excluding the at least two allocated sub-frames (there are 4 sub-frames remaining after the divided sub-frames are discounted; as such it is clear 16 is 2^4 times larger than 1).

With respect to claim 3, Ohtaka and Asano disclose, the electro-optical device according to claim 2 (see above).

Ohtaka further discloses, a sub-frame having the longest period (Sub4 period is 8 in fig. 7d) among the plurality of sub-frames excluding the at least two sub-frames being half as long as the sub-frames having the longest period among the plurality of sub-frames (8; clear this is half of 16 , which corresponds to the longest sub-field prior to being divided).

With respect to claim 4, Ohtaka and Asano disclose, the electro-optical device according to claim 1 (see above).

Ohtaka further discloses, the two sub-frames (SF1 and SF6 in fig. 7d) not being arranged consecutively in one frame of a period (clear from fig. 7d; col. 8, line 62 – col. 9, line 4).

With respect to claim 5, Ohtaka discloses, an electro-optical device, comprising:

a plurality of scanning lines (27 in fig. 4, for example);

a plurality of sustaining lines (28 in fig. 4, for example);

a plurality of electro-optical elements (col. 1, lines 4-10; col. 4, lines 33-36); and

a plurality of pixels, each of the plurality of pixels having an electro-optical element (col. 1, lines 4-10; col. 4, lines 33-36), brightness of each of the electro-optical elements being set for each of a plurality of sub-frames (col. 4, lines 36-48; fig. 7d), which constitute one frame of a period (1 field is equivalent to one frame) and each have a predetermined period (clear from fig. 7d), so that at least two levels of brightness can be set for one frame (col. 4, lines 44-48), and

lengths of the plurality of sub-frames excluding a sub-frame having a longest period (SF1 and SF6 in fig. 7d) being set to a period in binary weighted (col. 8, line 29, for example); and

the sub-frame having the longest period among the plurality of sub-frames being divided into at least two allocated sub-frames (col. 8, line 62 – col. 9, line 2), and

the plurality of sub-frames, which are set for a series of electro-optical elements among the plurality of electro-optical elements (col. 1, lines 9-10), the series of electro-optical elements being connected to a scanning and sustaining line (note the two x-axis electrodes per pixel in fig. 4), end substantially simultaneously (clear from fig. 7d that the sub-frame sustaining period (grayed area) ends simultaneously).

Ohtaka does not expressly disclose a plurality of data lines, a pixel circuit nor connecting two scanning lines to the series of electro-optical elements.

Asano discloses, an electro-optical device, comprising:

a plurality of scanning lines (127 in fig. 4);

a plurality of data lines (133 in fig. 4);

a plurality of electro-optical elements (121 in fig. 3); and

a plurality of pixel circuits (131 in fig. 4) to drive the plurality of electro-optical element, each of the plurality of pixel circuits having a first transistor (124 in fig. 3) and a storage capacitor (123 in fig. 3) to store a data signal (col. 3, lines 23-30) supplied via a data line (128 in fig. 3) among the plurality of data lines and the first transistor (clear from fig. 3); wherein the electro-optical elements are connected to at least two scanning lines (127A-B in fig. 3). Asano further discloses, that the data signal stored in the capacitor sets the brightness of the pixel (col. 2, lines 33-51; also note col. 3, lines 20-29).

At the time of the invention it would have been obvious to one of ordinary skill in the art to replace the addressing and pixel circuitry of Ohtaka with the pixel circuit and scanning lines of Asano.

The motivation for doing so would have been to achieve a high image contrast and high response speed (Asano; col. 1, lines 43-44).

With respect to claims 6, Ohtaka and Asano disclose, the electro-optical device according to claims 5 (see above).

Ohtaka further discloses, the two sub-frames (SF1 and SF6 in fig. 7d) not being arranged consecutively in one frame of a period (clear from fig. 7d; col. 8, line 62 – col. 9, line 4).

With respect to claim 7, Ohtaka discloses, an electro-optical device, comprising:

a plurality of scanning lines (27 in fig. 4, for example);

a plurality of sustaining lines (28 in fig. 4, for example);

a plurality of electro-optical elements (col. 1, lines 4-10; col. 4, lines 33-36); and

a plurality of pixels, each of the plurality of pixels having an electro-optical element (col. 1, lines 4-10; col. 4, lines 33-36), brightness of each of the electro-optical elements being set for each of a plurality of sub-frames (col. 4, lines 36-48; fig. 7d), which constitute one frame of a period (1 field is equivalent to one frame) and each have a predetermined period (clear from fig. 7d), so that at least two levels of brightness can be set for one frame (col. 4, lines 44-48); and

the sub-frame having the longest period among the plurality of sub-frames being divided into at least two allocated sub-frames (col. 8, line 62 – col. 9, line 2), and

a sub-frame having the longest period among n (n denotes a natural number) sub-frames (SF4 in fig. 7d) of the plurality of sub-frames, excluding the at least two allocated sub-frames (SF1 and SF6; n is seen as 4), being set to 2^{n-1} times as long as a sub-frame having the shortest period (SF2 in fig. 7d) among the n sub-frames (SF4 is equal to $2^3=2^{4-1}$; sub1 is equal to 1) and brightness for the one frame can be set to 2^{n+1} levels (col. 8, lines 28-32 discusses the possibility of $32=2^{4+1}$ levels), and

the plurality of sub-frames, which are set for a series of electro-optical elements among the plurality of electro-optical elements (col. 1, lines 9-10), the series of electro-optical elements being connected to a scanning and sustaining line (note the two x-axis electrodes per pixel in fig. 4), end substantially simultaneously (clear from fig. 7d that the sub-frame sustaining period (grayed area) ends simultaneously).

Ohtaka does not expressly disclose a plurality of data lines, a pixel circuit nor connecting two scanning lines to the series of electro-optical elements.

Asano discloses, an electro-optical device, comprising:

a plurality of scanning lines (127 in fig. 4);

a plurality of data lines (133 in fig. 4);

a plurality of electro-optical elements (121 in fig. 3); and

a plurality of pixel circuits (131 in fig. 4) to drive the plurality of electro-optical element, each of the plurality of pixel circuits having a first transistor (124 in fig. 3) and a storage capacitor (123 in fig. 3) to store a data signal (col. 3, lines 23-30) supplied via a data line (128 in fig. 3) among the plurality of data lines and the first transistor (clear from fig. 3); wherein the electro-optical elements are connected to at least two scanning lines (127A-B in fig. 3).

At the time of the invention it would have been obvious to one of ordinary skill in the art to replace the addressing and pixel circuitry of Ohtaka with the pixel circuit and scanning lines of Asano.

The motivation for doing so would have been to achieve a high image contrast and high response speed (Asano; col. 1, lines 43-44).

With respect to claim 8, Ohtaka and Asano disclose, the electro-optical device according to claim 7 (see above).

Ohtaka further discloses, the two sub-frames (SF1 and SF6 in fig. 7d) not being arranged consecutively in one frame of a period (clear from fig. 7d; col. 8, line 62 – col. 9, line 4).

With respect to claim 11, Ohtaka discloses, an electro-optical device, comprising:

a plurality of scanning lines (27 in fig. 4, for example);

a plurality of sustaining lines (28 in fig. 4, for example);

a plurality of electro-optical elements (col. 1, lines 4-10; col. 4, lines 33-36); and

a plurality of pixels, each of the plurality of pixels having an electro-optical element (col. 1, lines 4-10; col. 4, lines 33-36), brightness of the electro-optical element being set for each of a plurality of sub-frames (col. 4, lines 36-48; fig. 7d), which constitute one frame (one field is equivalent to one frame) of a period and each have a predetermined period (clear from fig. 7d), so that at least 2^n levels of brightness (n=4; $2^4 \leq 32$ levels possible; col. 8, lines 28-32; col. 9, lines 2-4) can be set for one frame,

number of the plurality of sub-frames being n+1 or more (number of sub-frames in fig. 7d is $6 \geq 4+1$), and

the sub-frame having the longest period among the plurality of sub-frames being divided into at least two allocated sub-frames (col. 8, line 62 – col. 9, line 2), and

the plurality of sub-frames, which are set for a series of electro-optical elements among the plurality of electro-optical elements (col. 1, lines 9-10), the series of electro-optical elements being connected to a scanning and sustaining line (note the two x-axis electrodes per pixel in fig. 4), end substantially simultaneously (clear from fig. 7d that the sub-frame sustaining period (grayed area) ends simultaneously).

Ohtaka does not expressly disclose a plurality of data lines, a pixel circuit nor connecting two scanning lines to the series of electro-optical elements.

Asano discloses, an electro-optical device, comprising:

a plurality of scanning lines (127 in fig. 4);

a plurality of data lines (133 in fig. 4);

a plurality of electro-optical elements (121 in fig. 3); and

a plurality of pixel circuits (131 in fig. 4) to drive the plurality of electro-optical element, each of the plurality of pixel circuits having a first transistor (124 in fig. 3) and a storage capacitor (123 in fig. 3) to store a data signal (col. 3, lines 23-30) supplied via a data line (128 in fig. 3) among the plurality of data lines and the first transistor (clear from fig. 3); wherein the electro-optical elements are connected to at least two scanning lines (127A-B in fig. 3).

At the time of the invention it would have been obvious to one of ordinary skill in the art to replace the addressing and pixel circuitry of Ohtaka with the pixel circuit and scanning lines of Asano.

The motivation for doing so would have been to achieve a high image contrast and high response speed (Asano; col. 1, lines 43-44).

With respect to claim 12, Ohtaka and Asano disclose, the electro-optical device according to claim 11 (see above).

Ohtaka further discloses, a sub-frame having a longest period (SF4=8) among the plurality of sub-frames, excluding the at least two allocated sub-frames, being 2^{n-1} times (4=n from claim 11; 2^3=8) as long as a sub-frame having a shortest period (SF2=1).

With respect to claims 20-21, Ohtaka and Asano disclose, the electro-optical device according to claim 1 (see above).

Asano further discloses, the electronic element being a current-driven organic EL element (col. 1, lines 16-24).

With respect to claim 22, as claim 22 is nothing more than a method step claim having identical limitations to those recited in claim 4. Therefore claim 22 is rejected on the same merits shown above in claims 1 and 4.

With respect to claim 23, as claim 23 is nothing more than a method step claim having identical limitations to those recited in claim 6. Therefore claim 23 is rejected on the same merits shown above in claims 5 and 6.

With respect to claim 24, as claim 24 is nothing more than a method step claim having identical limitations to those recited in claim 8. Therefore claim 22 is rejected on the same merits shown above in claims 7 and 8.

With respect to claim 30, Ohtaka and Asano disclose, the electro-optical device according to claim 1 (see above).

Ohtaka further discloses, an electronic apparatus (col. 1, lines 4-11), comprising: an electro-optical device.

6. Claims 13-15 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohtaka et al. (US 6,151,000) in view of Asano (US 6,975,290) and further in view of Wakitani et al. (US 5,940,142).

With respect to claim 13, Ohtaka discloses, an electro-optical device, which is capable of setting at least two levels of brightness for one frame (col. 4, lines 44-48), the electro-optical device comprising:

a plurality of scanning lines (27 in fig. 4, for example);

a plurality of sustaining lines (28 in fig. 4, for example);

a plurality of electro-optical elements (col. 1, lines 4-10; col. 4, lines 33-36); and

electro-optical elements that are controlled to take either an ON state or an OFF state based on gray scale data for each of a plurality of sub-frames (col. 4, lines 35-47), which constitute one frame of a period and each have a predetermined period (clear from fig. 7d); and

the sub-frame having the longest period among the plurality of sub-frames being divided into at least two allocated sub-frames (col. 8, line 62 – col. 9, line 2).

Ohtaka does not expressly disclose, a plurality of data lines, a pixel circuit, connecting two scanning lines to the series of electro-optical elements, or that two of the plurality of sub-frames are controlled to always concurrently take either the ON state or the OFF state.

Asano discloses, an electro-optical device, comprising:

a plurality of scanning lines (127 in fig. 4);

a plurality of data lines (133 in fig. 4);

a plurality of electro-optical elements (121 in fig. 3); and

a plurality of pixel circuits (131 in fig. 4) to drive the plurality of electro-optical element, each of the plurality of pixel circuits having a first transistor (124 in fig. 3) and a storage capacitor (123 in fig. 3) to store a data signal (col. 3, lines 23-30) supplied via a data line (128 in fig. 3) among the plurality of data lines and the first transistor (clear from fig. 3); wherein the electro-optical elements are connected to at least two scanning lines (127A-B in fig. 3).

At the time of the invention it would have been obvious to one of ordinary skill in the art to replace the addressing and pixel circuitry of Ohtaka with the pixel circuit and scanning lines of Asano.

The motivation for doing so would have been to achieve a high image contrast and high response speed (Asano; col. 1, lines 43-44).

Wakitani discloses, at least two of the plurality of sub-frames (sub8a and sub8b) being controlled to always concurrently take either the ON state or the OFF state (col. 10, lines 38-40; also note the concurrent operation of sub8a/8b in fig. 3).

Ohtaka, Asano and Wakitani are analogous art because they are both from the same field of endeavor namely grayscale design and driving schemes for electro-optical devices.

At the time of the invention it would have been obvious to one of ordinary skill in the art to concurrently drive the allocated sub-frames of Ohtaka, as taught by Wakitani.

The motivation for doing so would have been to provide a unique gray-scale value (16 in Ohtaka's case) that allows for additional gradations in the driving of the display.

With respect to claim 14, Ohtaka, Asano and Wakitani disclose, the electro-optical device according to claim 13 (see above).

Ohtaka discloses, the at least allocated two sub-frames having the same period of length (SF1 = SF6 is clear from fig. 7d; col. 8, line 62 – col. 9, line 2).

With respect to claim 15, Ohtaka, Asano and Wakitani disclose, the electro-optical device according to claim 13 (see above).

Ohtaka further discloses, the two sub-frames (SF1 and SF6 in fig. 7d) not being arranged consecutively in one frame of a period (clear from fig. 7d; col. 8, line 62 – col. 9, line 4).

With respect to claim 26, as claim 26 is nothing more than a method step claim having identical limitations to those recited in claims 11-15. Therefore claim 26 is rejected on the same merits shown above in claims 11-15.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to William L. Boddie whose telephone number is (571) 272-0666. The examiner can normally be reached on Monday through Friday, 7:30 - 4:30 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on (571) 272-3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

2/16/07
wlb

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SUPERVISORY PATENT EXAMINER